CLAIMS

1. A power semiconductor device having a main current carrying transistor section integrated with a sense current carrying transistor section for carrying a current which is smaller than and indicative of the current carried by the main current carrying section, wherein the main transistor section and the sense transistor section have a common first main electrode connected to a first main terminal of the device, wherein the main transistor section and the sense transistor section have separate second main electrodes with the second main electrode of the main transistor section connected to a second main terminal of the device and the second main electrode of the sense transistor section connected through a current sensing resistance to said second main terminal of the device, wherein the main transistor section and the sense transistor section have separate control electrodes, wherein control means includes comparison means for comparing a reference voltage defining a current limit value with the voltage across the current sensing resistance and providing a first control signal, wherein the first control signal is coupled to the control electrode of the sense transistor section, wherein the first control signal is coupled to further control means which provides a second control signal coupled to the control electrode of the main transistor section, and wherein the further control means comprises adjustment circuit means coupled to the first control signal and to the voltage across the current sensing resistance and arranged to provide the second control signal such that the second control signal is effective to maintain the voltage between the control electrode and the second main electrode of the main transistor section equal to the voltage between the control electrode and the second main electrode of the sense transistor section.

2. A device as claimed in claim 1, wherein the second control signal provided by the adjustment circuit means is connected indirectly to the control

electrode of the main transistor section as a third control signal via a buffer driver circuit.

3. A device as claimed in claim 2, wherein the buffer driver circuit includes an operational amplifier, a non-inverting input of this operational amplifier being connected to the second control signal voltage, and an inverting input of this operational amplifier being connected to its output and to the control electrode of the main transistor section, and wherein the comparison means includes an operational amplifier, a non-inverting input of this operational amplifier being connected to the current limit defining reference voltage, an inverting input of this operational amplifier being connected to the second main electrode of the sense transistor section, and the output of this operational amplifier being connected to the control electrode of the sense transistor section.

Subseq 4. A device as claimed in claim 2 or claim 3, wherein the adjustment circuit means includes an operational amplifier, first and second equal value resistors and a transistor, wherein a non-inverting input of this operational amplifier is connected to the voltage across the current sensing resistance, wherein one end of said first resistor is connected to the second main terminal of the device and the other end of said first resistor is connected to an inverting input of this operational amplifier and to a first main electrode of this transistor, wherein one end of said second resistor is connected to the first control signal voltage and the other end of said second resistor is connected to a second main electrode of this transistor which provides the second control signal, and wherein the output of this operational amplifier is connected to a control electrode of this transistor.

5. A device as claimed in claim 1, wherein the adjustment circuit means is a differential amplifier circuit, and wherein the second control signal

is provided by the differential amplifier circuit and is connected directly to the control electrode of the main transistor section.

6. A device as claimed in claim 5, wherein the differential amplifier circuit includes an operational amplifier, wherein a non-inverting input of this operational amplifier is connected to a junction in a first resistive divider which is provided between the first control signal voltage and the second main terminal of the device, wherein an inverting input of this operational amplifier is connected to a junction in a second resistive divider which is provided between the output of this operational amplifier and the voltage across the current sensing resistance, and wherein the output of this operational amplifier provides the second control signal.

7. A device as claimed in claim 5 or claim 6, wherein the comparison means includes an operational amplifier, wherein a non-inverting input of this operational amplifier is connected to the current limit defining reference voltage, wherein an inverting input of this operational amplifier is connected to the voltage across the current sensing resistance, and wherein the output of this operational amplifier provides the first control signal.

8. A device as claimed in any preceding claim, wherein the main transistor section comprises a power MOSFET or IGBT.

9. A device as claimed in any one of claims 1 to 8, wherein, within an encapsulation for the device, the main transistor section, the sense transistor section, the control means and the further control means are provided as a single integrated circuit chip.

10. A device as claimed in any one of claims 1 to 8, wherein, within an encapsulation for the device, the main transistor section and the sense

transistor section are provided as a first integrated circuit chip, and wherein the control means and the further control means are provided as at least one second integrated circuit chip.